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10/682,154	10/10/2003	Saichirou Kaneko	50195-391	8202

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	**Application No.** 10/682,154	**Applicant(s)** KANEKO ET AL.
	Examiner Thomas L Dickey	**Art Unit** 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.
4a) Of the above claim(s) *4-7 and 10-19* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-3,8,9 and 20-23* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *10 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a)☒ All b)☐ Some * c)☐ None of:
1.☒ Certified copies of the priority documents have been received.
2.☐ Certified copies of the priority documents have been received in Application No. _____.
3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date *10/10/03 and 03/15/04*.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kencke et al. 6,313,487 is cited because it appears to anticipate certain claims drawn to a non-elected embodiment. Note that SiGe layer 24 has a narrower band gap than Si substrate 10 and drain 12, while carrier-supplying source 14 is stacked above narrow band gap layer 24.

Election/Restriction

2. Applicant's election without traverse, on 30 September 2004, of the first embodiment, shown in figures 1 and 3A-3H and page 12 line 5 through page 23 line 4, is acknowledged. Applicant asserts that claims 1-3, 6-14 and 20-23 read on the first embodiment. Concerning this assertion the examiner makes the following findings:

A. Claim 6 requires that the reception layer comprise two parts, to wit, 1) a heavily doped region and 2) a drift region having a impurity-doping level lower that the heavily doped region. However, applicant's first embodiment has a reception layer comprising only a single part, drift region 20. Note application, figures 1 and 3H. Consequently, claim 6 does not read on applicant's first embodiment.

B. Claim 7 requires that the carrier-supplying region be stacked on the barrier-forming layer. However, in applicant's first embodiment the carrier-supplying region 18 and the barrier-forming layer 60 are laminated on the top surface of the reception layer 20, in a substantially same planar level. Note application, figures 1 and 3H. With the carrier supplying region 18 and the barrier forming layer 60 being at substantially the same planar level, it is not possible, in embodiment 1, for the carrier-supplying region to be stacked on the barrier-forming layer. Consequently, claim 7 does not read on applicant's first embodiment.

C. Claims 10 and 11 require that the barrier-forming layer be buried in the reception layer. However, applicant's first embodiment has the barrier-forming layer 60 laminated on the top surface of the reception layer 20. Note application, figures 1 and 3H. With the barrier-forming layer 60 laminated on the top surface of the reception layer 20, it is impossible, in embodiment 1, for the barrier-forming layer to be buried in the reception layer. Consequently, claims 10 and 11 do not read on applicant's first embodiment.

D. Claims 12-14 require that the gate-insulating film be spatially isolated from the top surface of the reception layer by the barrier-forming layer. However, in applicant's first embodiment, gate-insulating film 30 is in contact with (not spatially isolated from) the top surface of reception layer 20. Note application, figures 1 and 3H. Consequently, claims 12-14 do not read on applicant's first embodiment.

Claims 1-3,8,9 and 20-23 are readable onto elected embodiment 1, claims 1, 20, and 23 being generic (readable onto all embodiments). Claims 4-7 and 10-19 are withdrawn from consideration.

Oath/Declaration

3. The oath/declaration filed on 10/10/2003 is acceptable.

Drawings

4. The formal drawings filed on 10 October 2003 are acceptable.

Priority

5. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

6. The Information Disclosure Statements filed on 10/10/03 and 03/15/04 have been considered.

Claim Objections

7. Claim 23 is objected to because of the following informalities:

Claim 23, as presented, ends in a semicolon. It is assumed that this is a typo. Applicant is reminded that the statute requires each claim to end in a period (full stop).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 1-3 and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by HOSHI (5,939,754).

With regard to claims 1-3,21, and 22, Hoshi discloses a tunnel-injection device, comprising a reception layer 20 made of a first semiconductor (SiC); a barrier-forming layer 4 made of a second semiconductor (single crystalline silicon) having a band gap-narrower than the first semiconductor (SiC), a gate insulating film 7 disposed on the barrier-forming layer 4; a gate electrode 11 disposed on the gate insulating film 7; a carrier receiving region 21, comprising the first semiconductor (SiC), being contact with the reception layer 20, configured to receive the carriers injected by tunneling through the barrier; and a carrier supplying region 6, comprising the second semiconductor (single crystalline silicon) and having the same conductivity type, more highly doped, as reception layer 20, being in contact with the barrier-forming layer 4, configured to supply the carriers to the barrier-forming layer 4; the barrier-forming layer 4 being in metallurgical contact with the reception layer 20; the gate electrode 11 being configured (through insulator 8) to control the width of the barrier generated at the interface between the reception layer 20 and the barrier-forming layer 4 so as to change the tunneling probability of carriers through the barrier.

With regard to claim 23, Hoshi discloses a tunnel-injection device, comprising means for forming a heterojunction so as to generate a band-edge discontinuity barrier at the interface of the heterojunction, said means being a reception layer 20 made of a first semiconductor (SiC), in metallurgical contact with a barrier-forming layer 4 made of a second semiconductor (single crystalline silicon) having a band gap-narrower than the first semiconductor (SiC), means, said means being a carrier supplying region 6, for supplying carriers so as to accumulate the carriers at the interface of the heterojunction; means, said means being insulator 8 and gate electrode 11, for applying electric field to the band-edge discontinuity barrier so as to change the tunneling probability of the carriers through the band-edge discontinuity barrier; and means, said means being a carrier receiving region 21, for receiving carriers injected through the band-edge discontinuity barrier by tunneling.

Note figures 2 and 3 and column 4 lines 45-67, column 5 lines 1-14 and 55-67, and column 6 lines 1-12 of Hoshi.

B. Claims 1, 3, and 20-23 are rejected under 35 U.S.C. § 102(b) as being anticipated by THAPAR ET AL. (5,753,938).

With respect to claim 20, Thapar et al. discloses a method for fabricating a tunnel-injection device comprising the steps of preparing a base body 16 made of a first semiconductor (SiC); growing a layer 118 made of a second semiconductor (polysilicon) having a band gap narrower than the first semiconductor (SiC) on a surface of the base body 16; doping first impurity atoms in the layer so as to form a barrier-forming layer 28; doping selectively second impurity atoms with heavier doping level than the barrier-forming layer 28 so as to form a carrier supplying region 18, configured to supply carriers to the barrier-forming layer 28; depositing a gate insulating film 26 on the barrier-forming layer 28; and forming a gate electrode 36 on the gate insulating film 26, the gate electrode 36 is configured to control the width of the barrier generated at the interface between the base body

16 and the barrier-forming layer 28 so as to change the tunneling probability of carriers through the barrier.

With respect to claims 1, 3, 21, and 22, Thapar et al. discloses a tunnel-injection device with a reception layer 16 made of a first semiconductor (SiC); a barrier-forming layer 28 made of a second semiconductor (polysilicon) having a band gap-narrower than the first semiconductor (SiC), a gate insulating film 26 disposed on the barrier-forming layer 28; a gate electrode 36 disposed on the gate insulating film 26; a carrier receiving region 20, comprising the first semiconductor (SiC), being contact with the reception layer 16, configured to receive the carriers injected by tunneling through the barrier; and a carrier supplying region 18 being in contact with the barrier-forming layer 28, configured to supply the carriers to the barrier-forming layer 28; the barrier-forming layer 28 being in metallurgical contact with the reception layer 16; the gate electrode 36 being configured to control the width of the barrier generated at the interface between the reception layer 16 and the barrier-forming layer 28 so as to change the tunneling probability of carriers through the barrier.

With respect to claim 23, Thapar et al. discloses a tunnel-injection device with means for forming a heterojunction so as to generate a band-edge discontinuity barrier at the interface of the heterojunction, said means being a reception layer 16 made of a first semiconductor (SiC), in metallurgical contact with a barrier-forming layer 28 made of a second semiconductor (polysilicon) having a band gap-narrower than the first semiconductor (SiC), means, said means being a carrier supplying region 18, for supplying carriers so as to accumulate the carriers at the interface of the heterojunction; means, said means being a gate insulating film 26 and a gate electrode 36, for applying electric field to the band-edge discontinuity barrier so as to change the tunneling probability of the carriers through the band-edge discontinuity barrier; and means, said means being a carrier receiving region 20, for receiving carriers injected through the band-edge discontinuity barrier by tunneling.

Note figures 1,2,3A-3C, column 4 lines 1-23 and 55-67, and column 5 lines 1-48 of Thapar et al.

C. Claims 1, 8, 9, and 21-23 are rejected under 35 U.S.C. 102(b) as being anticipated by PEIN (5,378,912).

With regard to claims 1, 8, 9, and 21-22, Pein discloses a tunnel-injection device, comprising a reception layer 42a made of a first semiconductor (SiC); a barrier-forming layer 28 made of a second semiconductor (single crystalline silicon) having a band gap narrower than the first semiconductor (SiC), a gate insulating film 34 contacting the top surface of the reception layer 42a in a window part of the barrier-forming layer 28, being laminated on the top surface of the reception layer 42a and disposed on the barrier-forming layer 28; a gate electrode 36 disposed on the gate insulating film 34; a carrier receiving region 30 being contact with the reception layer 42a, configured to receive the carriers injected by tunneling through the barrier; and a carrier supplying region 26 in contact with the barrier-forming layer 28, laminated on the top surface of the reception layer 42a in substantially same planar level as the barrier-forming layer 28, and configured to supply the carriers to the barrier-forming layer 28; the barrier-forming layer 28 being in metallurgical contact with the reception layer 42a; the gate electrode 36 being configured to control the width of the barrier generated at the interface between the reception layer 42a and the barrier-forming layer 28 so as to change the tunneling probability of carriers through the barrier.

With regard to claim 23, Pein discloses a tunnel-injection device, comprising means for forming a heterojunction so as to generate a band-edge discontinuity barrier at the interface of the heterojunction, said means being a reception layer 42a made of a first semiconductor (SiC), in metallurgical contact with a barrier-forming layer 28 made of a second semiconductor (single crystalline silicon) having a band gap narrower than the first semiconductor (SiC), means, said means being a carrier supplying region 26, for supplying carriers so as to accumulate the carriers at the interface of the heterojunction; means, said means being a gate insulating film 34 and a gate electrode 36, for applying electric field to the band-edge discontinuity barrier so as to change the tunneling probability of the carriers through the band-edge discontinuity barrier; and means, said means being a carrier receiving region 30, for receiving carriers injected through the band-edge discontinuity barrier by tunneling.

Note figure 2 and column 21 lines 5-41 of Pein.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLD
11/04

Minhloan Tran
Primary Examiner
Art Unit 2826